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Question Paper Code : X 67548

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Sixth Semester
Electronics and Communication Engineering
CS 1358 – COMPUTER ARCHITECTURE
(Common to Seventh Semester-Electrical and Electronics Engineering)
(Regulations 2008)

Time : Three Hours Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Give the sequence of micro operations associated with push and pop operation.
2. Show the block diagram of the hardware that implements the following register transfer statement $yT_2 : R_2 \leftarrow R_1, R_1 \leftarrow R_2$.
3. What is meant by fast adder ?
4. Fast Multiplication techniques speed up the multiplication operation. How ?
5. Define the bussess designed in a processor.
6. What are the advantages of pipelining ?
7. Draw the SRAM cell diagram.
8. What is the need to include the cache memory ?
9. Differentiate Isolated IO and Memory Mapped IO.
10. What is SCSI ?

PART – B **(5×16=80 Marks)**

11. a) i) With a neat block diagram explain the basic operational concepts. **(8)**
    ii) Explain what is Big – Endian and Little – Endian. **(8)**

(OR)

b) i) What are the different bus structures available ? Describe it. **(8)**
    ii) Describe the different addressing modes with example. **(8)**

12. a) i) With flowchart, necessary block diagram, explain the arithmetic and subtraction operation's algorithm. **(8)**

ii) Discuss in detail about Booth multiplication algorithm. **(8)**

(OR)

b) i) Explain in detail about division algorithm. **(8)**

ii) Derive an algorithm for evaluating the square root of binary fixed point number. **(8)**

13. a) i) Draw and explain the block diagram of a Simple Processor model with Single-bus organization of the datapath inside a processor. **(10)**

ii) Briefly describe the Hardwired Control unit organization with a neat block diagram. **(6)**

(OR)

b) Write detailed notes on Instruction Hazards caused by Unconditional Branches. **(16)**

14. a) i) Describe the construction and working of a typical semiconductor ROM. **(8)**

ii) Discuss the performance consideration for cache memories. **(8)**

(OR)

b) i) Explain the need and role of cache memories in computers. **(7)**

ii) What are the requirements for memory management ? Explain any one memory management technique in detail. **(9)**

15. a) With neat diagrams explain the Connection of I/O Bus to CPU and Connection of I/O Bus to One Interface.

(OR)

b) Explain Direct Memory Access with a neat block diagram.

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